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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/798,943	LEE, JONG-JOO	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☒ Claim(s) *17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments, filed 3/19/2007, with respect to the rejection(s) of claim(s) 1-17 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Bai. Please note that the Bai reference has been reinterpreted; in making the rejection herein the examiner has labeled part 211a as the "connecting pad" and part 211b as the "terminal pad".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 7, and 9-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al (U.S. Patent #6326700), in view of Cady et al (U.S. Patent #6576992).

With respect to **claim 1**, Bai teaches an area array type package comprising: a substrate having a first face and a second face opposing the first face (Fig. 1, 21), there being a plurality of terminal pads (Fig. 1, 211b) and a plurality of connecting pads (Fig. 1, 211a) formed on the second face, and a

semiconductor chip attached to the first face of the substrate and electrically connected to the terminal pads and the connecting pads (Fig. 1, 20); the substrate further including first wirings connected to the terminal pad and providing electrical paths coupling the semiconductor chip and the terminal pads (Fig. 1, 22), and second wirings connected to the terminal pad and providing electrical paths coupling the semiconductor chip and the connecting pads (Fig. 1, 211); but does not teach at least one flexible cable having a plurality of conductive patterns thereon extending around at least one side edge of a lower one of at least two stacked packages, and electrically coupling the connecting pads of the packages through the conductive patterns. Cady teaches a stacked package (Fig. 1) having a flexible cable with a plurality of conductive patters thereon extending around a side edge of the lower package (Fig. 1, 30), and electrically coupling the connecting pads of each package (Fig. 1, 24). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a flexible cable to a stacked configuration of the package of Bai as taught by Cady in order to create a distributed capacitance intended to reduce noise in the device (Col 5 Ln 39-48).

With respect to **claim 2**, Bai teaches that the chip is a center pad type chip (Fig. 1).

With respect to **claim 3**, Bai teaches that the substrate further has first wirings (Fig. 1, 22) providing electrical paths coupling the semiconductor chip

and the terminal pads and second wirings (Fig. 1, 211) providing electrical paths coupling the semiconductor chip and the connecting pads.

With respect to **claim 4**, Bai teaches that the semiconductor chip is an edge pad type chip (Fig. 8).

With respect to **claim 7**, Bai teaches that the connecting pads are arranged in a straight row near an edge of the substrate (Fig. 2, 240).

With respect to **claim 9**, Bai does not teach a plurality of external connection terminals formed on the terminal pads of a lowermost package of the package. Cady teaches a plurality of external connection terminals on the lowermost package of a stacked device (Fig. 1, 36). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide external connection terminals on the device of Bai as taught by Cady in order to connect the stacked device to other devices.

With respect to **claims 10 and 13**, Bai does not teach a non-conductive adhesive layer interposed between adjacent device packages. Cady teaches an adhesive layer between the individual packages (Fig. 2, 40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide an adhesive layer between stacked devices in order to improve the planarity of the module (Col 5 Ln 53).

With respect to **claim 11**, Bai teaches that the area array type is a BGA package (Col 1 Ln 14).

With respect to **claim 12**, Bai teaches providing a first individual package of an area array type (AAT) having a substrate with a first face and a second face opposing the first face (Fig. 1, 21), a plurality of terminal pads (Fig. 1, 211b) and a plurality of connecting pads (Fig. 1, 211a) formed on the second face; the substrate further including first wirings connected to the terminal pad and providing electrical paths coupling the semiconductor chip and the terminal pads (Fig. 1, 22), and second wirings connected to the terminal pad and providing electrical paths coupling the semiconductor chip and the connecting pads (Fig. 1, 211); but does not teach a flexible cable; wherein the plurality of connecting pads are electrically connected to conductive patterns on the flexible cable; bending the flexible cable to extend around at least one side edge of the package; and stacking a second individual AAT package having a substrate with a first face and a second face opposing the first face, a plurality of terminal pads and a plurality of connecting pads formed on the second face on the first AAT package, wherein the plurality of connecting pads are electrically connected to the conductive patterns on the flexible cable. Cady teaches a stacked package (Fig. 1) having a flexible cable with a plurality of conductive patters thereon extending around a side edge of the lower package (Fig. 1, 30), and electrically coupling the connecting pads of each package (Fig. 1, 24). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a flexible cable to a stacked configuration of the package of Bai as taught by Cady

in order to create a distributed capacitance intended to reduce noise in the device (Col 5 Ln 39-48).

With respect to **claim 14**, Bai teaches a plurality of external connection terminals under the first package (Fig. 1, 240).

With respect to **claim 15**, Bai teaches providing a first package of an area array type (AAT) having a substrate with a first face and a second face opposing the first face (Fig. 1, 21), a plurality of terminal pads (Fig. 1, 211b) and a plurality of connecting pads (Fig. 1, 211a) formed on the second face; the substrate further including first wirings connected to the terminal pad and providing electrical paths coupling the semiconductor chip and the terminal pads (Fig. 1, 22), and second wirings connected to the terminal pad and providing electrical paths coupling the semiconductor chip and the connecting pads (Fig. 1, 211), but does not teach that the plurality of connecting pads are electrically connected to conductive patterns on a flexible cable; forming an adhesive layer under the first package; attaching a second AAT package having a substrate with a first face and a second face opposing the first face, a plurality of terminal pads and a plurality of connecting pads formed on the second face to the first package by the adhesive layer; and bending the flexible cable to extend around at least one side edge of the second AAT package wherein the plurality of connecting pads are electrically connected to the conductive patterns on the flexible cable. Cady teaches a stacked package (Fig. 1) with an adhesive layer between the individual packages (Fig. 2, 40), having a flexible cable with a plurality of conductive patters

thereon extending around a side edge of the lower package (Fig. 1, 30), and electrically coupling the connecting pads of each package (Fig. 1, 24). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide an adhesive layer between stacked devices in order to improve the planarity of the module (Col 5 Ln 53), and to provide a flexible cable to a stacked configuration of the package of Bai as taught by Cady in order to create a distributed capacitance intended to reduce noise in the device (Col 5 Ln 39-48).

With respect to **claim 16**, Bai teaches that the first wirings are formed on the second face of the substrate (Fig. 1, 22).

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bai and Cady, in view of Taniguchi et al (U.S. Patent #6388333).

With respect to **claims 5 and 6**, Bai teaches does not teach that the second wirings including vias providing electrical paths coupling the chip and the connecting pads. Taniguchi teaches wiring including vias (Fig. 6, vias are formed in the solder resist 10) in immediate proximity to the connecting pads (Fig. 6, 5) coupling the chip and connecting pads. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the substrate of Bai with vias formed in a solder resist as taught by Taniguchi in order to form the solder balls on the wiring with more precision.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bai and Cady, in view of Takashima et al (U.S. Patent #6160313).

With respect to **claim 8**, Bai does not teach that the connecting pads are arranged in a staggered row near an edge of the substrate. Takashima teaches connecting pads that arranged in a staggered row near an edge of a substrate (Fig. 9, 32C). It would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange the connecting pads of Bai in a way as taught by Takashima in order to implement wire bonding with a high accuracy.

Allowable Subject Matter

Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

bps

EVAN PERT
PRIMARY EXAMINER